# High Performance Data Bus Encoding Technique in DSM Technology

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***Abstract*— To increase the performance and reliability of highly integrated circuits like DSP processors, Microprocessors and SoCs, transistors sizes are continues to scale towards Deep Submicron and Very Deep Submicron dimensions . As more and more transistors are packed on the chip to increase the functionality more metal layers are being added to the integrated chips. Hence the performance of the chips depends more on the performance of global interconnect and on-chip busses than gate performance. The performance of the global interconnects and on-chip data busses is limited by switching activity, energy dissipation and noise such as crosstalk, leakage, supply noise and process variations etc. which are the side effects of the technology scaling. To increase the performance of overall system it is necessary to control and reduce these technology scaling effects on on-chip data buses. One of the favorable techniques to increase the efficiency of the data buses is to encode the data on the on-chip bus. Data encoding technique is the promising method to increase the performance of the data bus and hence overall system performance. Hence high performance data bus encoding technique is propose which reduces switching activity, transition energy dissipation, crosstalk and crosstalk delay. The proposed method reduces the switching activity by around 23%, energy dissipation by 46%, 6C, 5C and 4C type crosstalk by around 89%, 73% and 31% respectively and crosstalk delay by around 44% to 50% compare to unencoded data.**

***Index Terms*— Switching activity, energy dissipation, crosstalk, crosstalk delay, Deep submicron SoCs, reliability, interconnects, data bus**

## I. Introduction

Traditional gate centric design of CMOS circuits has paved the way to interconnect centric design as more and more metal layers are being added to the chip. Hence the performance of the global interconnects and buses became a deciding factor for the performance of overall system. Energy dissipation and crosstalk noise are main challenges on the data buses which transmit signals between the different functional blocks or sub systems Unfortunately in nanometer and sub nanometer technologies the inter wire capacitance dominates the substrate capacitance and its magnitude is several times larger than load capacitance. The power consumption of on-chip wiring occupies a significant portion of total chip power consumption. In fact it is about 50% of total chip power consumption [1]. It has been estimated that more than 30% of on-chip wiring power consumption is due to data buses and long interconnects and that fraction is growing with technology scaling. The characteristics features of data buses and long interconnects such as wire spacing [2], wire width, wire length, coupling length, wire material, driver strength and signal transition time, etc. influences the coupling effect. This increased inter wire effect on on-chip buses and on long interconnects not only increase the energy dissipation but also deteriorate the signal integrity due to the inter wire or coupling capacitance. As the VLSI technology progress towards deep submicron and very deep submicron technologies crosstalk affects the reliability and delay of the signal transmission over on-chip data buses. Hence it is very important design challenge reduce the energy dissipation as well as the affects of crosstalk on on-chip data buses.

## II. Energy Dissipation On Data Buses

Data buses and Interconnect design play an important role in modern VLSI systems by providing a communication medium between long distant points having low latency, small energy consumption, reliable and robustness against different noise mechanisms. An important figure of merit for data buses and long interconnects is the energy consumption [3], which depends on bus topology, routing materials and technology parameters. The approximate energy expression for the self transitions and coupling transitions considering lumped model of the bus is analyzed by Sotiriadis and Chandrakasan [4]. For the 3-bit data bus the same lumped model is considered here. Energy expression for 3-bit data bus can be expressed as

$$E_1 = C_L\{(1+\lambda)(V_1^f - V_1^i) - \lambda(V_2^f - V_2^i)\}V_1^f . \quad (1)$$

$$E_2 = C_L\{-\lambda(V_1^f - V_1^i) + (1+2\lambda)(V_2^f - V_2^i)\} - \lambda(V_3^f - V_3^i) . \quad (2)$$

$$E_3 = C_L\{-\lambda(V_2^f - V_2^i)\} + (1+\lambda)(V_3^f - V_3^i)V_3^f . \quad (3)$$

$$E = E_1 + E_2 + E_3 . \quad (4)$$

where $V_1^f$ , $V_2^f$ and $V_3^f$ are final voltages and $V_1^i$ , $V_2^i$ and




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$V_3^i$ are the initial voltages of the 3-bit data bus wires respectively. $V_1^f, V_2^f, V_3^f, V_1^i, V_2^i$ and $V_3^i$ can be either $V_{dd}$ or Ground potential. Combining the equation.1, equation.2 and equation.3 the total energy can be calculated as in equation.4..E1, E2, and E3 represent energy for wires 1, 2 and 3, respectively. For a 0.18 nm CMOS technology and minimum distance between wires, the ratio of coupled capacitance ($C_I$) to substrate capacitance ($C_L$) is $\lambda = \frac{C_I}{C_L} = 3.2$ .[5] The energy saved due to the reduction of transitions is given in [5] as

$$\text{Energy saved} = \left(1 - \frac{E_{UNC}}{E_{COD}}\right) * 100 \qquad (5)$$

where $E_{UNC}$ is the energy dissipated due to unencoded data transitions and $E_{COD}$ is the energy dissipated due to coded data transitions.

The coupling capacitance not only depends on the spacing between bus wires but also on the data dependent transitions and the coupling effect will increase or decrease depending upon the relative switching activity between adjacent bus wires [5]. Hence reducing switching activity eventually reduces the energy dissipation. Switching activity or Transition activity on the data bus can be reduced by employing bus encoding techniques. Several bus encoding techniques have been proposed in the literature to reduce energy dissipation during bus transmission. These techniques mainly relay on reducing the data bus activity by decreasing self transitions or transitions due to inter wire or coupling capacitance. Reducing the energy dissipation transitions by encoding the data on the data buses leads to reducing the bus activity hence overall energy dissipation can be reduced.

Over the past few years, a number of data bus encoding schemes have been proposed for reducing the total transitions on on-chip data bus. For on-chip data buses, one popular coding scheme is the bus invert coding technique proposed by Stan and Burleson [6]. Other variants of the bus invert coding schemes include a decomposition approach [7] and partial bus coding technique [8]. The energy dissipated due to coupling capacitance is analyzed in [9-14]. For instruction buses Gray code [15], T0 code [16], the Beach code [17] have been proposed which reduces the transitions there by reducing the energy dissipation. In almost all above mentions methods either self transitions or coupling transitions are considered. All these methods are concentrated on only decreasing the energy dissipation on the on-chip buses but not considered the effect of crosstalk.

## III. Crosstalk And Crosstalk Delay

Number One of the important effects of coupling capacitances is that it may induce unwanted voltage spikes in neighboring bus wire. This is knows as Crosstalk. A wire on which a switching transition occurs is termed an *aggressor* and the wire on which it produces a noise spike is termed as a *victim*. Typically, an aggressor wire is physically adjacent to a victim wire and they may be modeled as being connected by a distributed coupling capacitance. Hence, a switching event in the aggressor wire while the victim wire is silent can result in the injection of at current into the victim wire, causing an electrical spike. However, a large coupling capacitance relative to the self-capacitance of the wire can cause a large inadvertent spike on the victim that may cause a spurious switching event, potentially leading to errors on victim wire and increased delay due to charging and discharging. The analytical delay on on-chip data buses in deep sub-micron has been proposed by Sotiriadis et al.[18]. The crosstalk can be classified into six types 1C, 2C, 3C, 4C, 5C and 6C according to the $C_C$ of two wires in 3-bit interconnect bus models [2].

The crosstalk has become a major concern because of continuing scaling of dimensions of wires. The propagation delay of data buses and interconnects caused by self capacitance, coupling capacitance and resistance is becoming prominent than gate delay [19]. This crosstalk causes delay faults and introduces errors on Data buses and interconnects which degrades the reliability and performance of the integrated circuits. Hence the performance and reliability of the chip depends more on performance of interconnects and data buses than logic performance. In literature many techniques are proposed to reduce or to avoid the crosstalk. Crosstalk delay faults can be reduced by reducing the coupling transitions [5].The total energy consumption and delay which determines maximum speed of the bus depends on crosstalk as given in [10],[20].

Crosstalk delay results due to charging and discharging of a coupling capacitance of data bus. Reducing the transition activity on the on-chip data buses is the one of the attractive way of reducing the crosstalk which intern reduces crosstalk delay. On of the simplest method to eliminate crosstalk is by using passive shielding [21]. However it requires twice the number of wires which results to a 100% area overhead. However instead of inserting shield wire between every pair of wires the spacing between the wires can be increased which can decrease the coupling transitions. Even then the area overhead is 100% [22]. A bus encoding technique is proposed which can avoid forbidden patterns i.e. the patterns of 010 and 101. Avoiding forbidden patterns can eliminate class 6 crosstalk. But this technique requires 52-bus lines for 32-bit data bus [20]. Crosstalk preventing coding (CPC) can able to eliminate some of the crosstalk classes. For 32-bit bus it requires 46-bit bus [23] hence large area overhead. A bus encoding technique is proposed for SoC buses to eliminate opposite transitions and to minimize power. It requires 55-bit bus for 32-bit data bus [24]. Selective shielding technique is proposed [25] which eliminates opposite transitions on adjacent bus lines. It also requires 48-bit bus for 32-bit data bus. Dual-rail coding technique is proposed in [26] which send both the original as well as duplicated data bits which are placed adjacently. This technique also requires 100% area


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overhead. Crosstalk delay as well as reliability and/or power consumption problem of interconnects are considered and proposed Joint coding scheme in [27-28]. Crosstalk avoidance CODEC design is proposed in [29] by using Fibaonacci number system. Recently ECC has been employed on data buses to transfer data reliably. Hence these busses are called Fault tolerant buses [30]. In recent days it is discovered that encoding the data on data bus can reduces the some classes of crosstalk with much low area overhead compare to the shielding techniques and others. Transition activity on the data bus can be reducing by employing bus encoding techniques. Several bus encoding techniques have been proposed to reduce power consumption during bus transmission in literature. These techniques mainly relay on reducing the data bus activity. Reducing power consuming transition by encoding the data on the data buses leads to reducing the bus activity hence overall power consumption is reduced [6],[11-14],[31]. However these techniques are not evaluated their performance for the crosstalk delay. The proposed technique not only reduces the power consuming transitions but also crosstalk and delay due to crosstalk. It requires only 2 extra bus bit for any data bus width.

## IV. High Performance Data Bus Evcoding Scheme

The proposed data bus encoding technique called Bus regrouping with hamming distance (BRG-HD) is based on reduction of switching activity occurring on data bus when a new data is to be transmitted. By implementing the following algorithm performance and reliability of the data bus can be increased. The proposed algorithm for 16-bit Data bus (Db) is given as follows:

Let 16-bit data bus is represented by Db [0:15]

$Db_0\ Db_1\ Db_2\ Db_3\ Db_4\ Db_5\ Db_6\ Db_7\ Db_8\ Db_9\ Db_{10}\ Db_{11}\ Db_{12}\ Db_{13}\ Db_{14}\ Db_{15}$

- Calculate the total number of CT (coupling transitions) of the present data on data bus with the previous data.
- Calculate the total number of ST (Self transitions) of the present data on data bus with the previous data.
- Calculate the energy dissipation on data bus due to self and coupling transitions.
- Calculate 6C, 5C, 3C, 2C and 1C type crosstalk transitions and its delay on the data bus.
- If total CT >= (n/2) then
- Consider the grouping of the present bus data as follows
  Odd Group: $Db_0\ Db_2\ Db_4\ Db_6\ Db_8\ Db_{10}\ Db_{12}\ Db_{14}$
  Even Group: $Db_1\ Db_3\ Db_5\ Db_7\ Db_9\ Db_{11}\ Db_{13}\ Db_{15}$
- Calculate the Hamming Distance between odd group of present data and odd group of previous data. This is represented as HDOPD = Hamming distance of Odd position data bits.
- Calculate the Hamming Distance between even group of present data and even group of previous data. This is represented as HDEPD = Hamming distance of Even position data bits.
- Transmit the data on the data bus by following the below conditions:

If HDOPD > HDEPD, flip the data in odd bit positions and append bit '1' on the left and bit '0' on the right side of the encoded data. If HDEPD > HDOPD, flip the data in even bit right side of the encoded data.positions and append bit '0' on the left and bit '1' on the If HDOPD = HDEPD, flip the entire data and append bit '1' on the left and bit '1' on the right side of the encoded data.

- If total CT<n/2 is true then transmits the data as it is, append bit '0' on the left and bit '0' on the right side of the encoded data.
- Calculate the total transitions due coupling and self capacitance, energy dissipation, crosstalk and normalized crosstalk delay on transmitted encoded data with present transmitting encoded data.
- Calculate the efficiency of the above parameters.

## V. Experimental Results

The proposed encoding technique(BRG-HD) performance is compared with Bus invert(BINV)[6], Dynamic encoding technique (DYNAMIC)[11], Shift invert (SHINV)[31], Energy efficient spatial coding technique ( EESCT) [14] and A Novel deep submicron bus coding [13]. The simulations are performed on 8-bit, 16-bit, 32-bit and 64-bit data buses with three groups of 1000, 2000, 5000 and 10000 data vectors. Switching activity, Energy dissipation, Crosstalk and crosstalk delay are considered as metric parameters. Energy saved is calculated based on the expression given in [18] and for 180nm CMOS technology, $\lambda = 3.2$ [5]. It shown in Table I that the switching activity for 64-bit data bus has reduced by around 23% compared to unencoded data and it is better than other technique. Table II shows the reduction in energy dissipation. BRG-HD reduces the energy dissipation by around 46% compared unencoded data. It reduces around 1% to 34% compare with the other techniques. The proposed technique's efficiency is consistent with the increase of bus width as seen from Fig.1. Other technique's efficiency reduces with increase of bus width except for Novel coding. Fig.2 indicates that the BRG-HD technique is very effective in reducing the energy dissipation as the input sample size increases. Table III and Table IV shows the crosstalk reduction for 32-bit and 16-bit data bus respectively. It shows that BRG-HD is the efficient in reducing the worst case crosstalk types. BRG-HD reduces the 6C, 5C and 4C types by around 89%, 73% and 31% respectively for 32-bit data bus. These crosstalk types are converted to 3C, 2C and 1C type which are non critical crosstalk. Finally Table V shows that the proposed technique crosstalk delay is reduced by around 44% to 50%. Overall the proposed technique performance is very much better than other techniques.

## Conclusions

Since the technology is moving towards DSM and VDSM technology, the bus encoding techniques has to overcome the design challenges of present scenario. The proposed data bus encoding technique called Bus Regrouping with Hamming Distance (BRG-HD) is a high performance technique


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TABLE. 1. SWITCHING ACTIVITY REDUCTION (IN) OF DIFFERENT ENCODING TECHNIQUES FOR 64-BIT DATA BUS

| METHOD | Uncoded | Coded | Efficiency |
|---|---|---|---|
| BINV | 413427 | 388127 | 6.119581 |
| DYNAMIC | 413427 | 360717 | 12.74953 |
| NOVEL | 413427 | 316230 | 23.510076 |
| BRG-HD | 413427 | 315653 | 23.649641 |
| SHINV | 413427 | 370970 | 10.269528 |
| EESCT | 413427 | 382613 | 7.453311 |

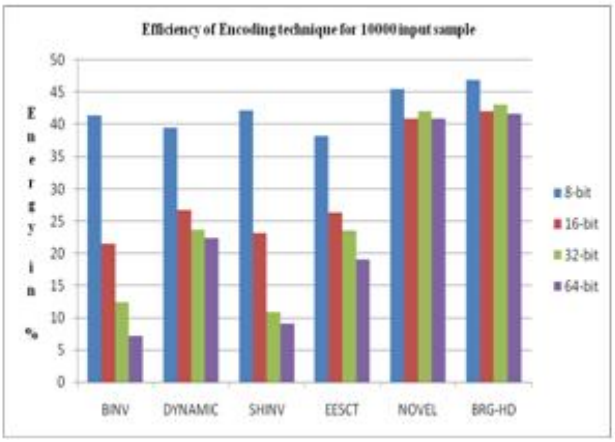


Figure. 1. Comparison of Energy Sissipation Efficiency of Different Dncoding Techniques for 10000 Inputs for Different Bus Widths

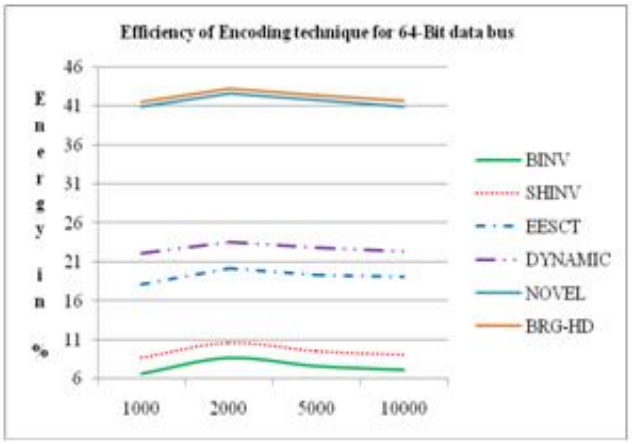


Figure. 2. Comparison of Energy Efficiency of Different Encoding Techniques for 64-bit Data Bus for Different Input Sample Sizes.

TABLE. II. ENERGY SAVED (IN %) OF DIFFERENT ENCODING TECHNIQUES

| METHOD | 8-bit | 16-bit | 32-bit | 64-bit |
|---|---|---|---|---|
| BINV | 41.41068 | 21.54488 | 12.38811 | 7.16344 |
| DYNAMIC | 39.55572 | 26.72299 | 23.65808 | 22.35502 |
| NOVEL | 45.55654 | 40.9542 | 42.0495 | 40.9707 |
| BRG-HD | 46.94077 | 42.0729 | 43.15248 | 41.63158 |
| SHINV | 42.2474 | 23.0923 | 10.88095 | 9.062785 |
| EESCT | 38.28969 | 26.32516 | 23.59237 | 19.07573 |

which reduces switching activity, energy dissipation, crosstalk and crosstalk delay which are main challenges of

TABLE. III. CROSSTALK REDUCTION (IN %) OF DIFFERENT ENCODING TECHNIQUES FOR 32-BIT DATA BUS

| METHOD | Class 6 | Class 5 | Class 4 | Class 3 | Class 2 | Class 1 |
|---|---|---|---|---|---|---|
| BINV | 8.69 | 22.23 | 35.35 | -0.95 | 32.02 | -25.16 |
| DYNAMIC | 87.56 | 30.82 | -0.47 | -208.6 | -82.16 | -9.49 |
| NOVEL | 87.40 | 68.24 | 19.36 | -308.5 | -1324 | -26.15 |
| BRG-HD | 89.27 | 73.85 | 31.50 | -299.9 | -1378 | -33.96 |
| SHINV | 20.85 | 16.29 | 20.07 | -62.26 | -76.02 | -25.69 |
| EESCT | 51.45 | 36.30 | 21.98 | -67.64 | -109.0 | -38.34 |

TABLE. IV. CROSSTALK REDUCTION (IN %) OF DIFFERENT ENCODING TECHNIQUES FOR 16-BIT DATA BUS

| METHOD | Class 6 | Class 5 | Class 4 | Class 3 | Class 2 | Class 1 |
|---|---|---|---|---|---|---|
| BINV | 45.03 | 7.02 | 34.54 | 52.61 | 74.45 | -28.98 |
| DYNAMIC | 88.73 | 25.05 | -22.38 | -66.29 | -18.10 | -8.51 |
| NOVEL | 89.31 | 54.52 | 14.01 | -217.35 | -397.7 | -32.21 |
| BRG-HD | 92.55 | 70.36 | 20.43 | -213.86 | -317.6 | -42.29 |
| SHINV | 60.53 | 17.27 | 15.58 | -30.87 | -49.81 | -41.99 |
| EESCT | 78.51 | 28.99 | -3.61 | -64.59 | 34.66 | -40.49 |

TABLE. V. CROSSTALK DELAY REDUCTION EFFICIENCY OF DIFFERENT ENCODING TECHNIQUES

| METHOD | 8-bit | 16-bit | 32-bit | 64-bit |
|---|---|---|---|---|
| BINV | 41.6125345 | 27.16235 | 22.549829 | 11.478879 |
| DYNAMIC | 39.270323 | 23.641127 | 26.286856 | 21.594661 |
| NOVEL | 42.8748117 | 37.482051 | 43.278483 | 41.494913 |
| BRG-HD | 44.0212021 | 46.88493 | 50.179608 | 44.798727 |
| SHINV | 39.6891276 | 25.52913 | 15.998213 | 12.722027 |
| EESCT | 34.3078751 | 28.045456 | 31.722654 | 22.792479 |

DSM and VDSM technologies. This technique is very useful in SoC and high performance complex systems.

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